New Delay Line Control System at the NPOI

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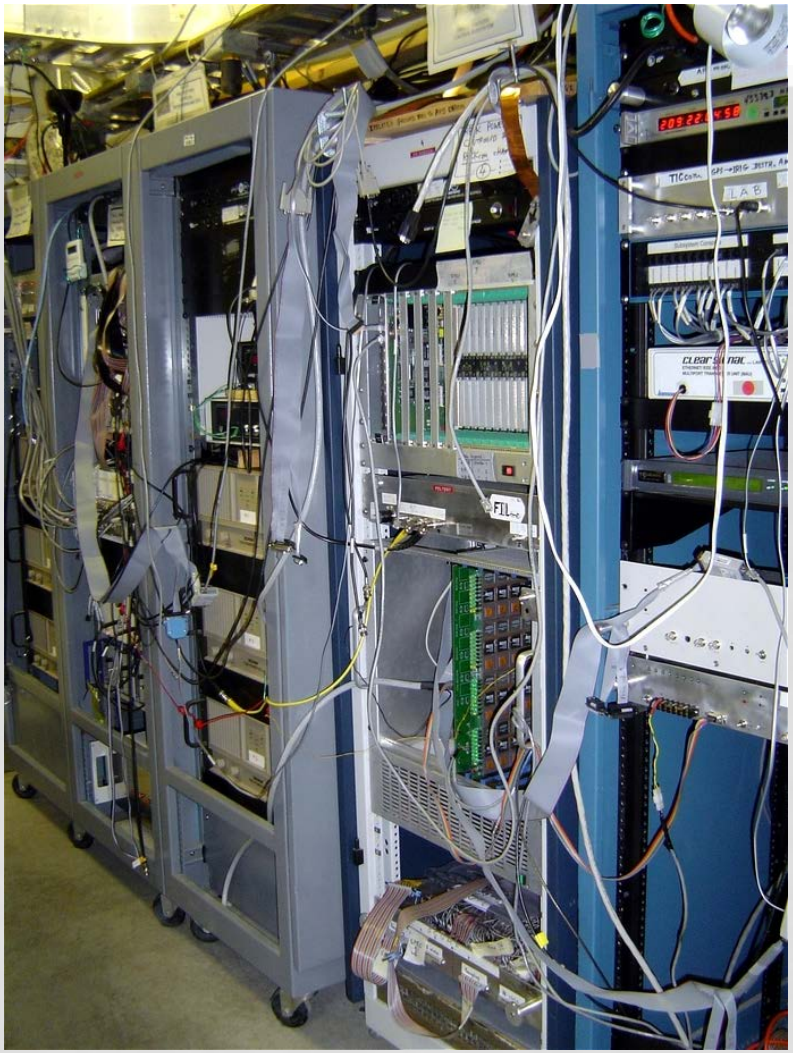
FAST DELAY LINE CONTROL SYSTEM



JPL's original FDL Controller

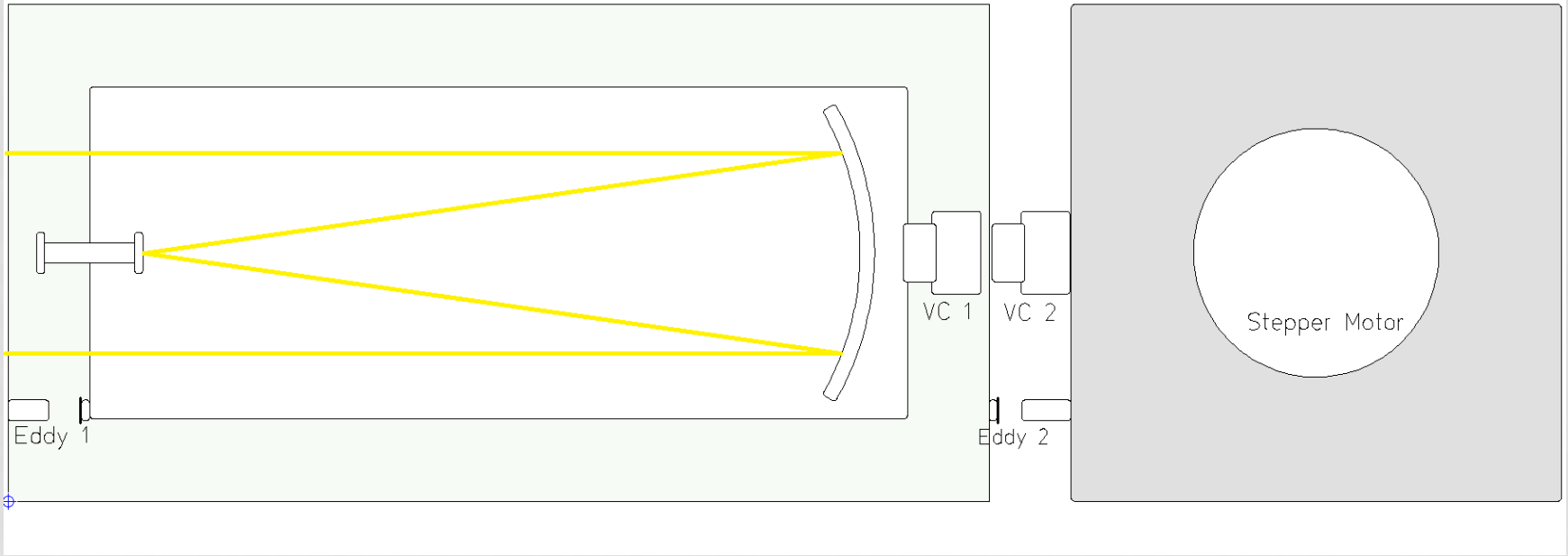
- First prototype developed 1991*[1]
- 50Mhz 68030 CPU's using VxWorks
- Problems with bus congestion
- Most parts deprecated
- Diagnostics difficult
- custom hardware makes repairs / replacements difficult

PC based FDL controller

- Use off-the-shelf components when possible
- In-system diagnostics and tuning abilities
- PC-based with Graphical User Interface support
- Application programming interface
- Cost effective

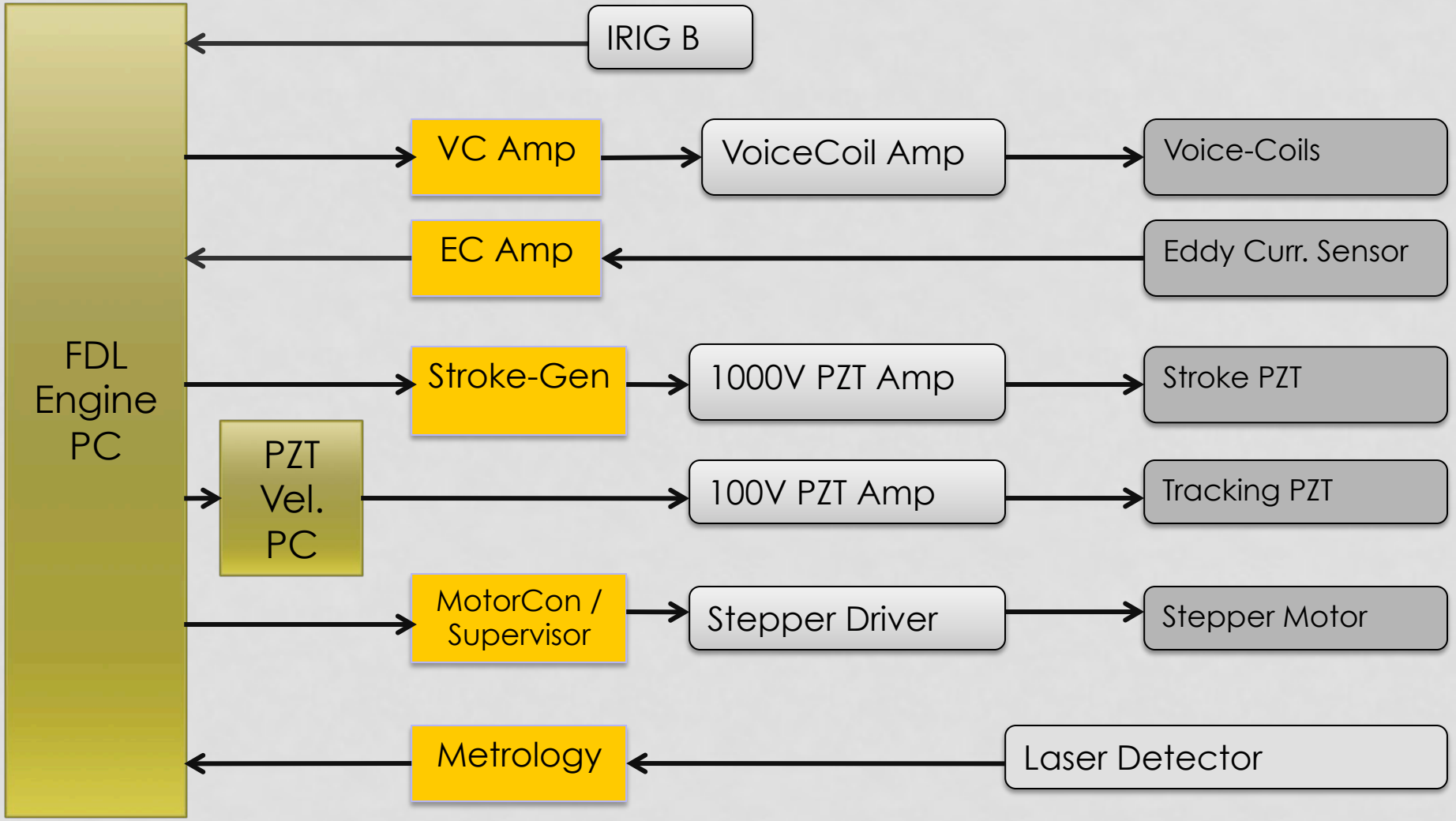
*[1]Prototype High Speed Optical Delay Line for stellar interferometry. Colavita, M.M., Hines, B.E., Shao, M., Klose, G.J. and Gibson, B.V. 1991, in Active and Adaptive Optical Systems, ed. M.A. Ealey, Proc. SPIE, SPIE (Bellingham), 1542, 205.

FDL CART



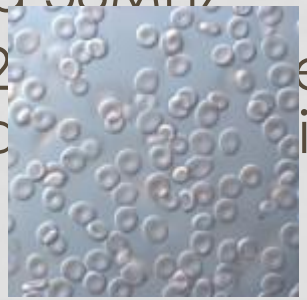
- PZT Servo stack (30µm/100V)
- Stroke modulator stack (5µm/100v)
- Voice Coil with acceleration 0.25m/s
- Eddy current sensors (non-contact displacement)
- Stepper-motor with micro-stepping driver on separate motor cart

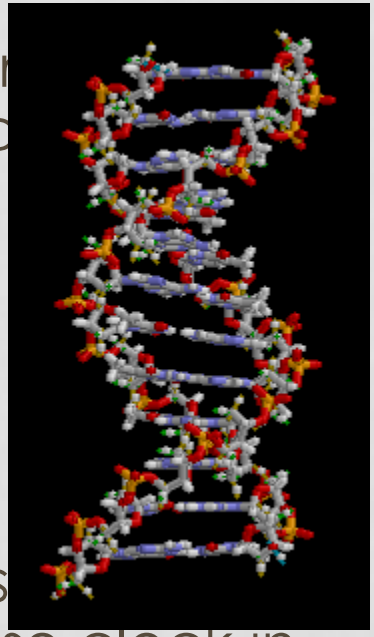
FDL CONTROLLER



METROLOGY

- Metrology is a heterodyne setup using opto-acoustical modulators with either 40MHz and 38Mhz
- Phase differences translate to a 2 e
  With a 633nm wavelength laser, c ic
  and $\lambda / 256$ resolution we obtain:





$$\Delta\lambda = \frac{633}{2*256} nm = 1.215nm$$

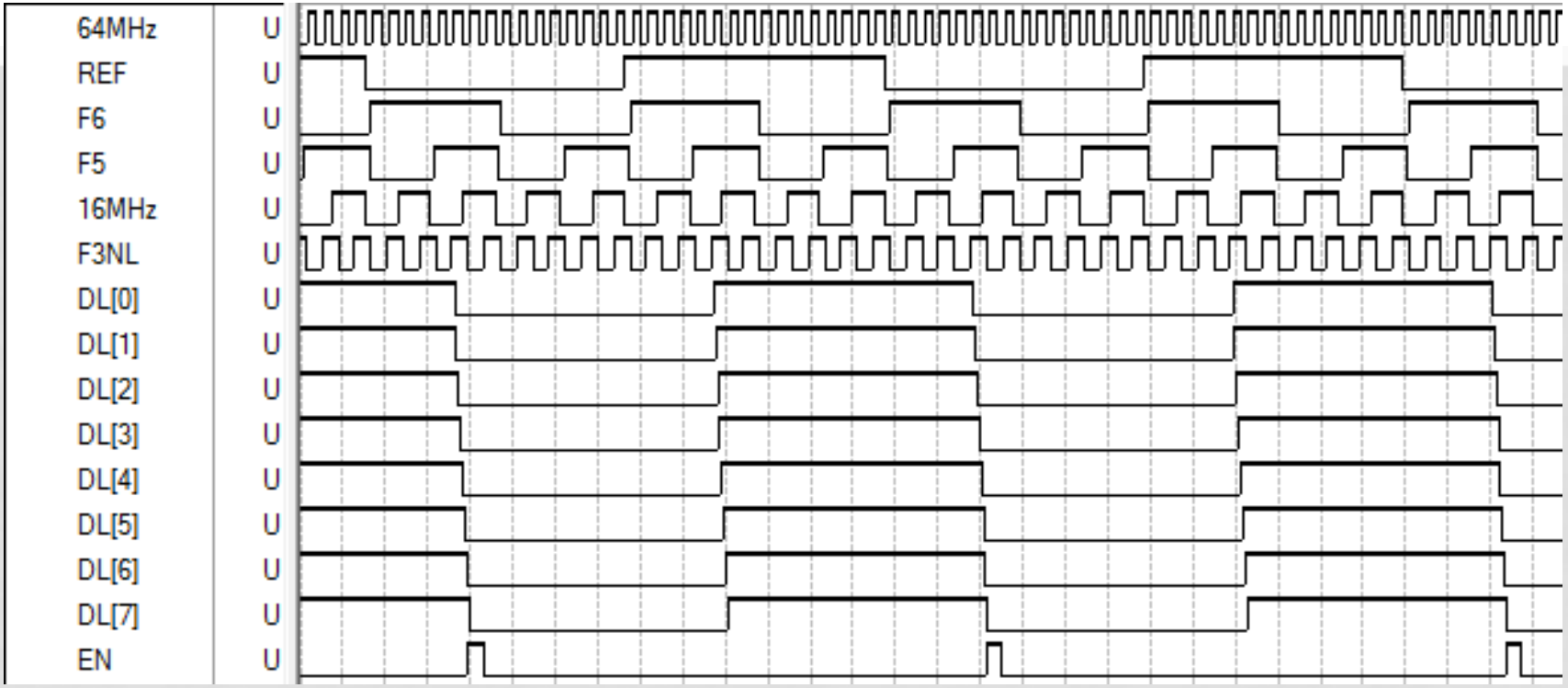
- JPL affectionately named it a nicron
- Detection of a 2MHz signal with $\lambda / 256$ with s
  precision is not trivial and would require a base clock in the GHz range.

Image Blood cells - NISE Network Image Collection, Kristina Yu, Exploratorium
Image DNA: brian0918 Wikipedia

METROLOGY DESIGN

- Detection occurs with Phase Locked Loop based clock multipliers. Using the 2MHz reference signal, 4/8/16/32/64 MHz clocks are created in phase with the reference signal and are latched when a 1 to 0 transition occurs on the unknown signal.
- We used a single FPGA implementation utilizing Altera's Stratix II, which has sufficient logic elements, speed and appropriate PLL's with high accuracy

METROLOGY PHASE DETECTION



Using above generated clocks, λ /32 can be detected. Using the heterodyne frequency of 2MHz, this results in 15.625ns precision. Higher resolutions are achieved by latching 8-tap monolithic delay lines with 2ns tap-to-tap delay.

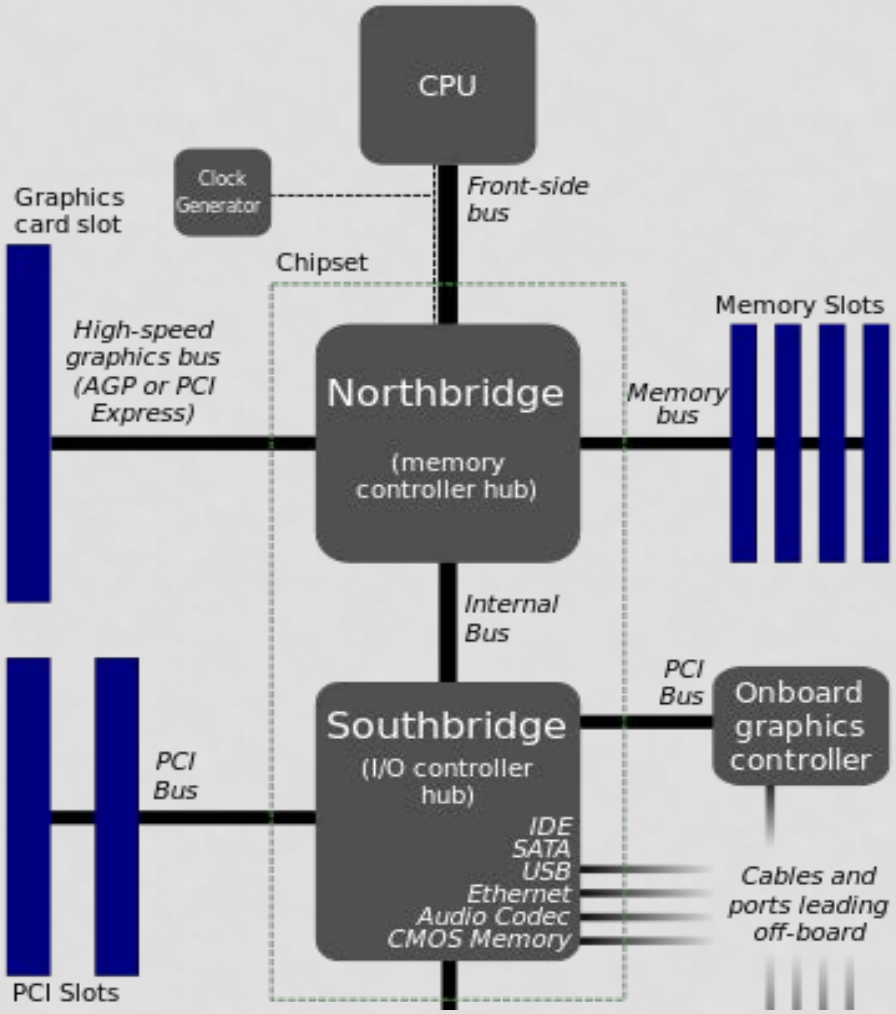
METROLOGY

- Interface requirements
  - High speed metrology position sampling for frequency response determination. Currently, 100kHz in system sampling is implemented
  - A recent position measure is required at a rate of 4kHz with low latency and jitter at single digit µs
  - The metrology is utilizing a high-speed DMA card with synchronous 16bit serial data transfer
    - Data rates were sufficient enough to allow several 10s of megabytes of data per second
    - But Linux did not play nice and jitter / latency were not sufficient for real-time control.

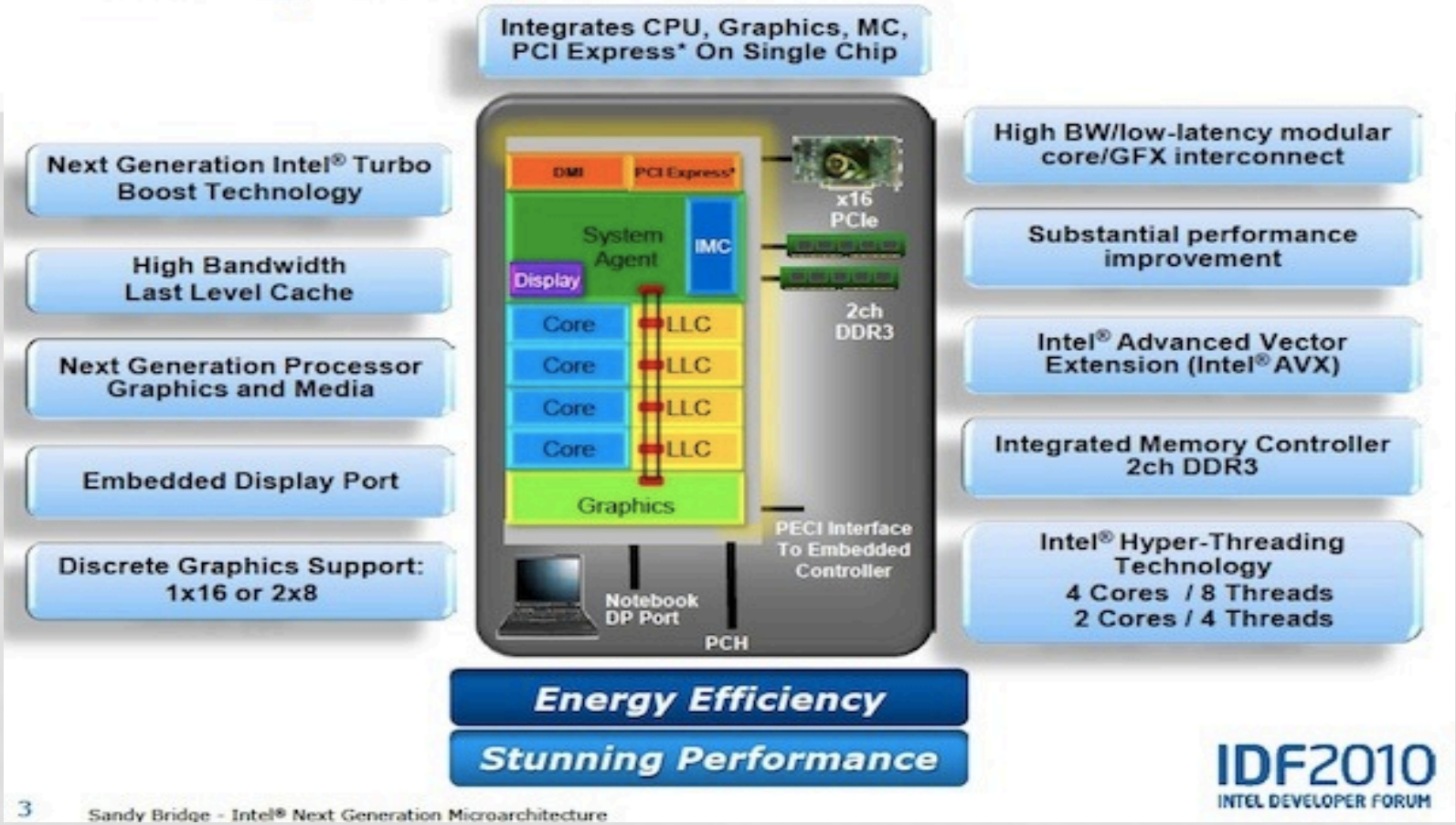
TIMING PROBLEMS

- Bus systems
  - Both PCI and PCI-E are not made for real-time deterministic data transfer.
  - Burst transfers especially for graphics cards can block the bus /kernel for ms
  - Poor interrupt control did not help either
- Linux real-time extensions guarantee deterministic scheduling, but that does not necessarily mean low-latency scheduling.
  - Kernel 2.6 has horrible low-latency mostly due to being non-preemptive
  - Drivers can (and tend to) block the kernel for up to several 100us

PREVIOUS INTEL ARCHITECTURE



www.intel.com



- Intel updated the ring-bus controller to integrate and connect all sub-cores, increased performance and efficiency and lower latency.

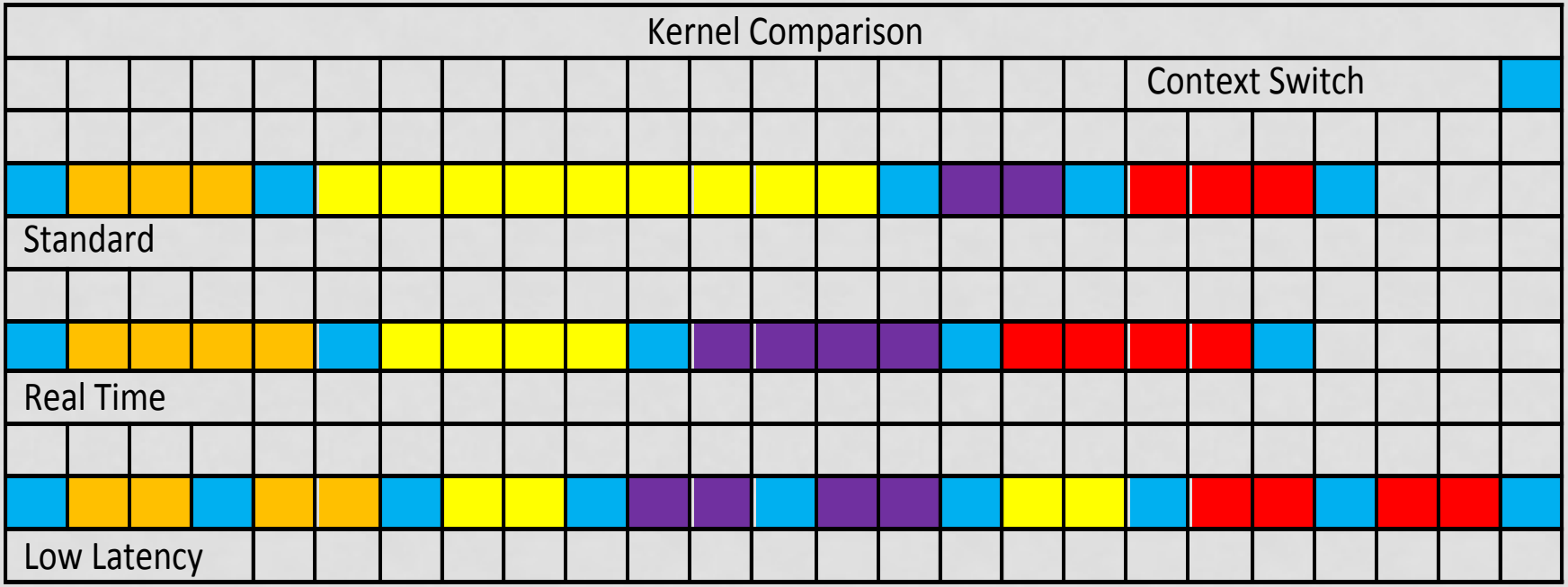
http://www.bit-tech.net/hardware/cpus/2010/04/21/intel-sandy-bridge-details-of-the-next-gen/1
http://www.intel.com/content/www/us/en/chipsets/mainstream-chipsets/h67-express-chipset.html

LOW LATENCY PATCHES

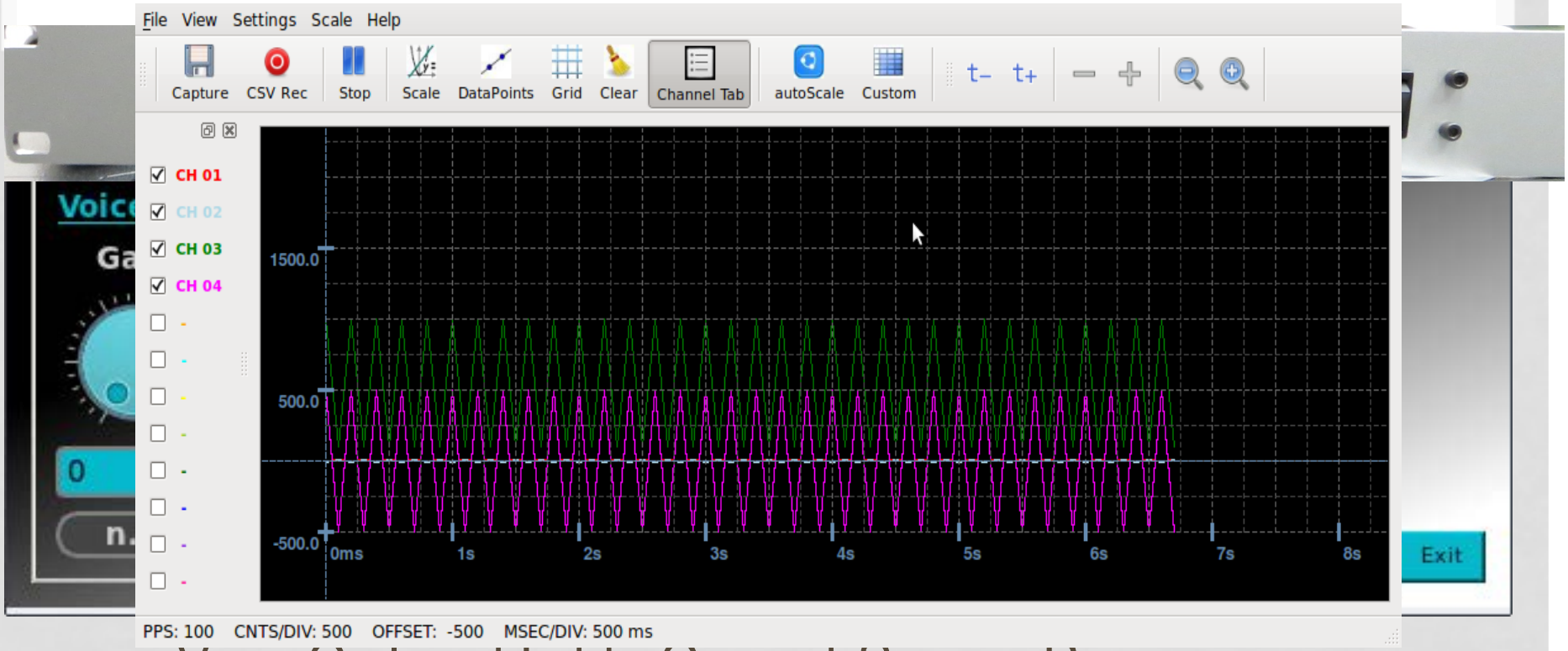
- Latency defined as the delay between the generation of an event and its realization.
- Real-time does not mean high throughput or low latency, it is about predictability
- Plethora of patches with different optimizations
- Low-latency patch (runs scheduler more often) rt-preempt patch makes kernel interruptible
- both patches were combined by Ingo Molnar - allows single digit ms latency and very low jitter
- Good low-latency kernels are provided by Planet CCRMA and Ubuntu Studio
- Drivers were optimized to allow low latency behavior

http://www.linuxdevcenter.com/pub/a/linux/2000/11/17/low_latency.html
http://ccrma.stanford.edu/planetccrma/software/understandlowlat.html
www.ubuntustudio.com

KERNEL SCHEDULING



IN SYSTEM TUNING/ DIAGNOSTICS

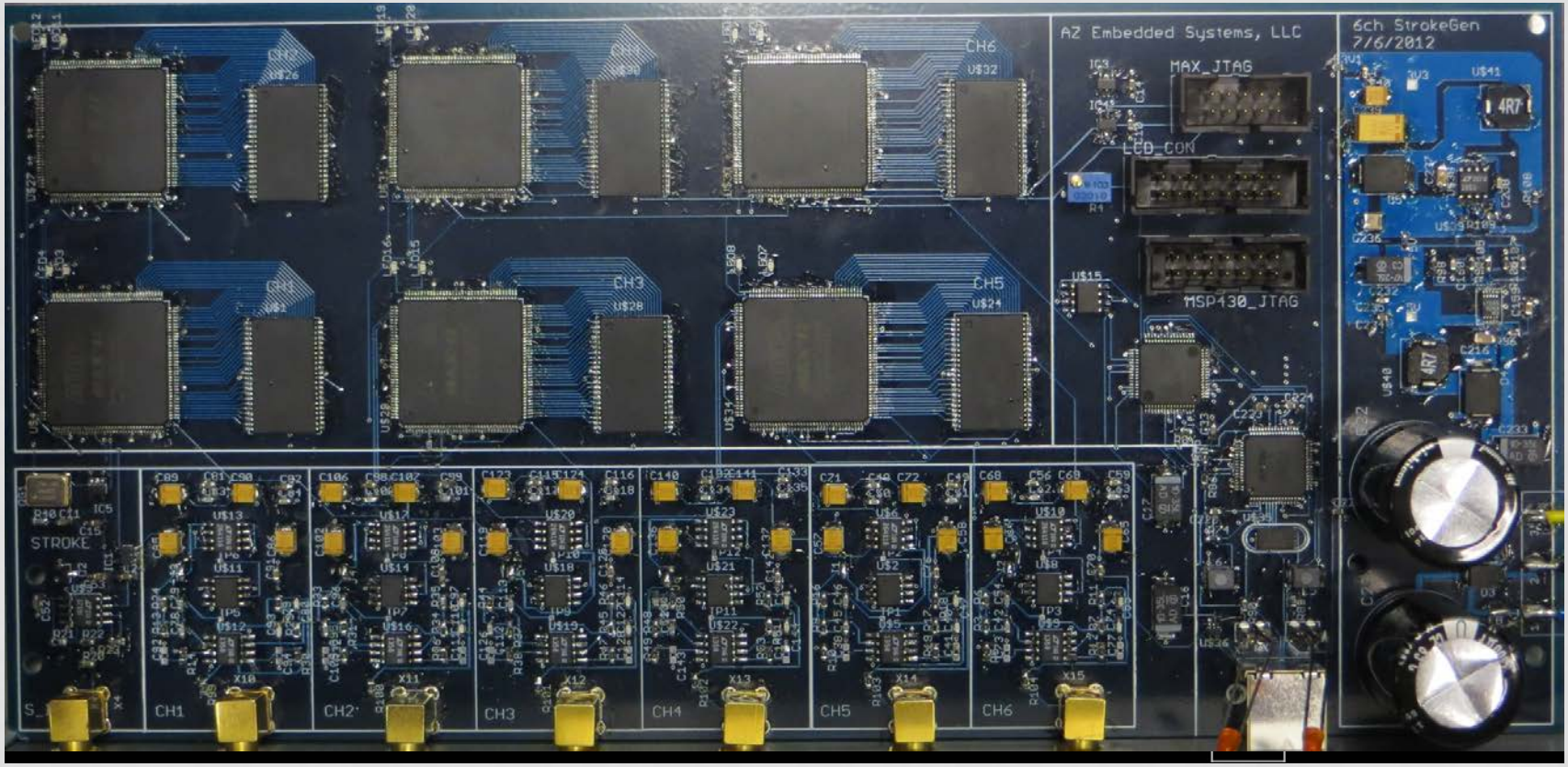


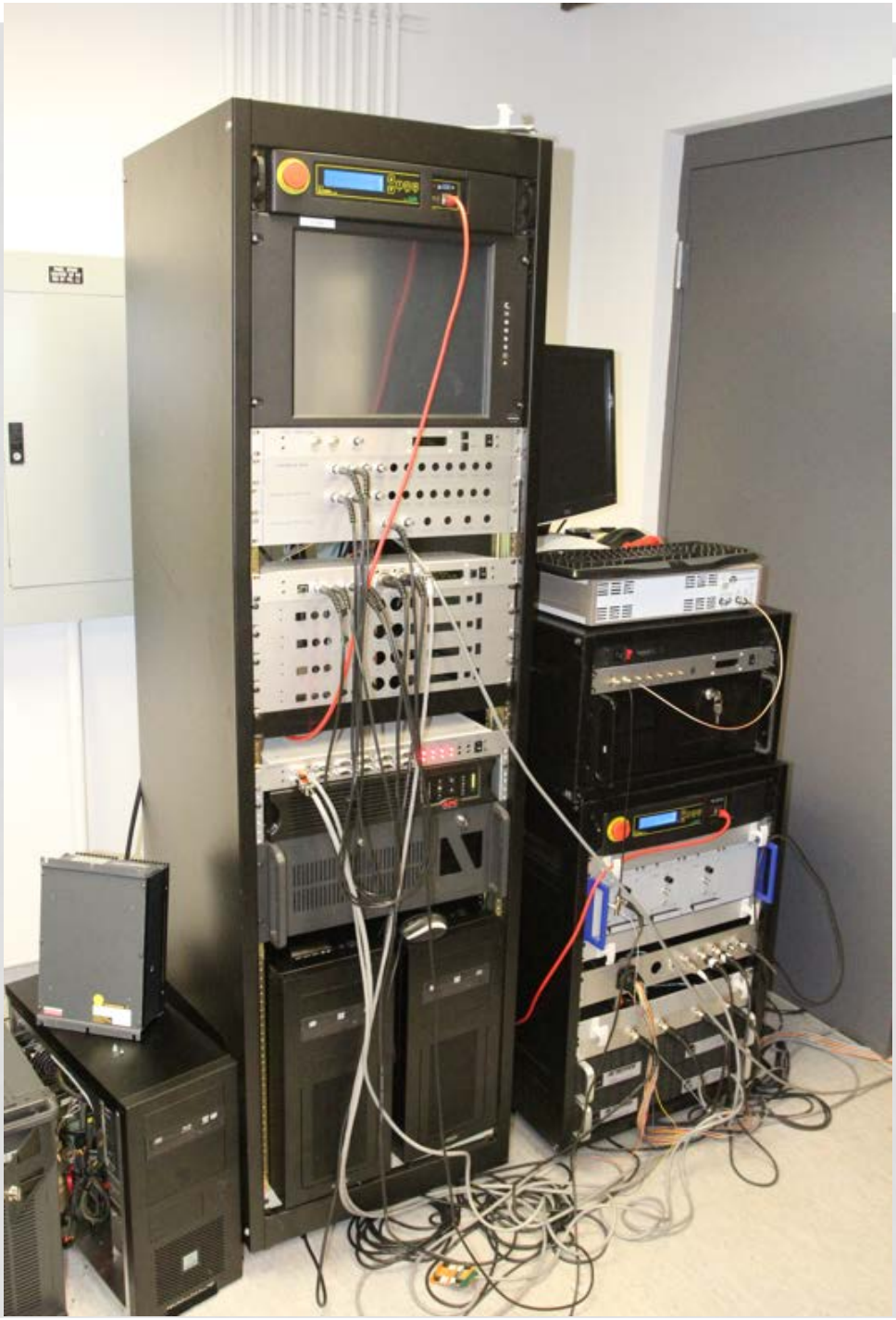
- VoiceCoil and Eddy-Current-Sensor Preamp
  - USB2.0 interface with Windows, Mac and Linux support
  - Programmable Voice-Coil Gain
  - Programmable Gain/Offset for Eddy-Current-Sensors
  - Full GUI support
  - Lead/lag compensation and signal conditioning to increase control stability

STROKE GENERATION

- 6ch Stroke Signal Generator
  - Modulator stack (5um, 1000V) used open-loop with lookup table for temporal modulation of interference fringe phase.
  - Most efficient sweep is a linear fringe sweep (triangular sweep).
  - Fast USB2.0 interface for instant waveform upload
  - Low-latency trigger input
  - 2000 16-bit samples per 2ms
  - Full parallel operation with arbitrary waveforms on all 6 channels
  - Full GUI support & full Application Programming Interface (API)
  - In-system synchronized position / stroke capture
  - Processing occurs via Python's numerical library (numpy) with DBUS interface

STROKE GENERATOR





PC-based FDL Control System

- Linux with 3.2 low-latency kernel
- In system diagnostic and tuning ability with 100kHz sampling of metrology position
- 2-3nm jitter variance in lab
- API for FDL control
- API for stroke linearization (sampling and signal generation)